Title: MEMORY DEVICE COMPRISING HYSTERETIC CAPACITANCE MEANS

Inventor: Yoh TAKANO-Appln. No.: Unknown Docket No.: 024808-00015

FIG.1

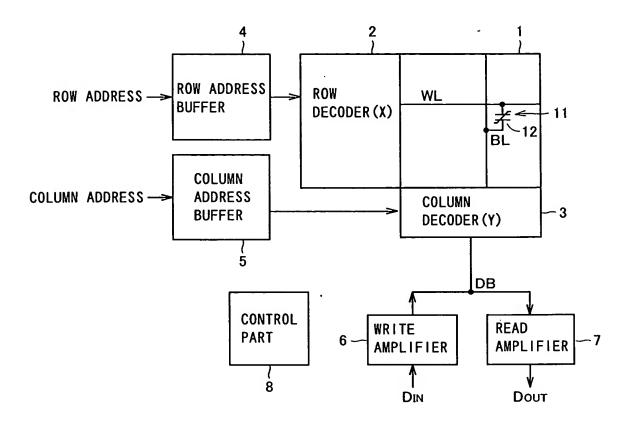
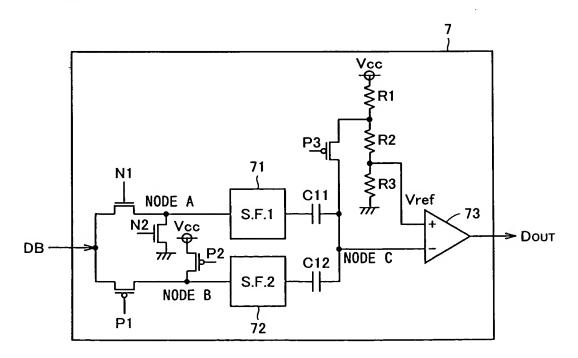


FIG.2



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FIG.3

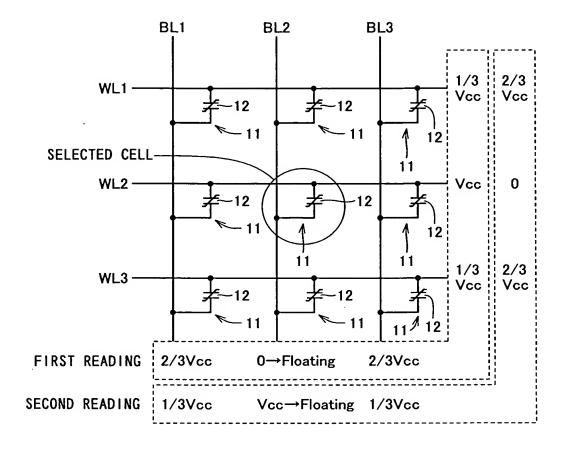


FIG.4

INITIAL DATA	FIRST VARIATION	DATA FOLLOWING FIRST READING	SECOND VARIATION		VARIATION CORRESPONDING TO TWO READ OPERATIONS
0	ΔVa	0	-∆V _b	1	ΔV_a - ΔV_b <0
1	ΔV _b	0	-ΔV _b	1	Δ V _b - Δ V _b =0

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FLOATING

FIG.5

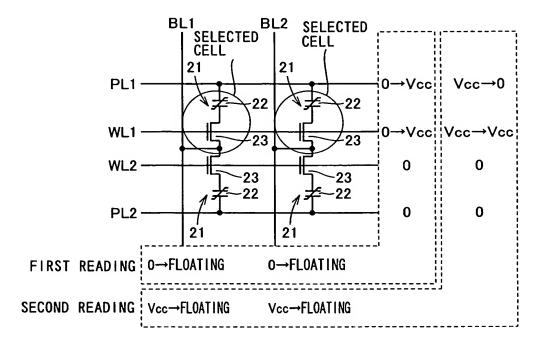
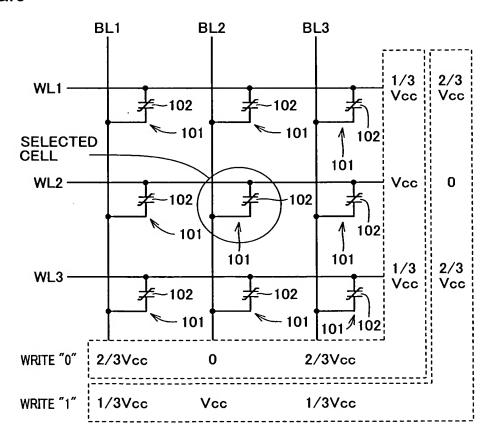


FIG.6



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FIG.7

